1. Suppose we want to implement the following logic equations.

\[ X = AB' + C(B+D) \quad Y = (A' + B)(AC + C'D) \quad Z = A \oplus B + CD' \]

(a) If these equations are implemented with a PROM, how many words must the PROM have and how many bits per word must it have?

(b) If these equations are implemented with a PLA, how many product terms must it have?

(c) If the equations are implemented with a PAL, how many product terms must it have?

2. Show how the sequential circuit shown below can be mapped onto a single configurable logic block. Do this by specifying the functions that the LUTs implement and showing the paths through the multiplexers that must be configured to provide the required connections (show this by drawing heavy lines on a photocopy of page 6-21 of the notes). Also show what values must be stored in each location of the LUTs to implement the required logic functions.
3. A 32K×8 SRAM chip is shown, below. Using this chip, design a memory system that has a total of 128 KB of memory and a memory width of 16 bits. Be sure to show all of the address and data lines as well as the control signals that you would need to use your RAM with a hypothetical processor.

![32Kx8 SRAM Diagram]

4. Consider the program on page 1-21 and 1-22 of the lecture notes. Suppose the simple processor is augmented with a direct-mapped instruction cache with 16 words. Each cache word includes a tag, consisting of the upper 12 bits of the stored instruction’s address and the instruction itself. Assume that all words in the cache are zero at the time the program starts execution. Show the contents of the cache the first time that the instruction at location 000a is executed. Show the contents of the cache the second time that the instruction at location 000a is executed. Show the contents of the cache the third time that the instruction at location 000a is executed.

Suppose that an instruction fetch takes 2 clock cycles for instructions that are present in the cache, but 10 clock cycles for instructions that are not in the cache. How much time is spent on instruction fetches during the first execution of the loop in the program on 1-21 and 1-22? How much time is spent on instruction fetches during the second execution of the loop? Explain your answers.

5. A 32K×8 RAM chip uses coincident decoding by splitting the internal decoder into row select and column select. (a) Assuming that the RAM cell array is square, what is the size of each decoder, and how many AND gates are required for decoding an address? (b) Determine the row and column selection lines that are enabled when the input address is the binary equivalent of 21000₁₀.
6. A DRAM has a refresh interval of 128 ms and has 4096 rows. What is the interval between refreshes for distributed refresh? What is the minimum number of address pins on the DRAM? If we used the minimum number of address pins, what would the word size of the DRAM be?