1. A sequential circuit has one flip flop $Q$, two inputs $X$ and $Y$ and one output $S$. The circuit consists of a full adder circuit connected to a $D$ flip flop as shown in Figure 4-36 in Mano and Kime. Derive the state table and state diagram for the sequential circuit.

2. Design a sequential circuit that determines if the number of 1s in an input data stream is divisible by 3 or not. Your circuit will have a data input $D$, an enable input $EN$ and a clock input. It will also have a single output $Z$. When $EN = 0$, $Z=1$. After $EN$ goes high, your circuit will observe the number of 1s in the incoming data stream and whenever the number of 1s seen so far is divisible by 3, the output $Z$, will be 1. At all other times it will be zero. The serial parity generator on page 4-9 of the notes performs a similar function.

   Create a state transition diagram for your circuit (it should have 3 states). Write down the output equation and the next state equations. Show a schematic that implements your design.

3. There is a keypad with three keys (labeled 1, 2 and 3) that is used as a combination lock. The combination for the safe is 1-2-3 (that is 1 then 2 then 3). You need to build a circuit that will have an output that is high when ever this sequence is pressed. Assume that the output from the keypad is a two-bit binary number equal to the value of the button pressed and zero (00) when no button is pressed. Design your circuit with D-type flip-flops and any other gates you need.
4. Assume that each flip-flop has a setup time of 2 ns, a hold time of 3 ns and a clock-to-output delay of 5 ns. Further assume that each gate has a delay of 2 ns except each inverter has a delay of 1 ns. What is the maximum clock frequency that you can clock the following circuits. Also discuss what constraints are placed on the inputs.

a. 

b. 

c.
5. A pair of signals, Request (R) and Acknowledge (A) are used to coordinate transactions between a CPU and an I/O system. These signals are synchronous with the clock and, for a transaction, are to always have their transitions appear in the order shown, below. Your job is to design a handshake checker circuit to check this I/O handshake scheme. The checker had inputs R and A as well as an asynchronous reset signal (RESET). The output is E=0 if the transitions are in order and E=1 if not. Once the output is 1, it will remain 1 until a RESET signal is seen.

In general, R comes first and is high for at least one clock cycle before A goes high. Once A goes high, both R and A can remain high for a long time. R must go low before A, however.

Write a VHDL description for this circuit and turn in your code and a simulation showing both a valid and invalid set of transitions.

```
CLK         ____________
R           ____________
A           ____________
E           ____________
RESET      ____________
```
6. Design a circuit that implements the following state diagram. Use D-type flip-flops and any other gates you need. There is one input and one output as shown. Also write VHDL for this circuit and simulate it. For the simulation, let the input start at zero (0) for two clocks and then set the input high for thirteen (13) clock cycles after which time it should go low (0) again. Turn in your VHDL source and simulation.