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**Abstract**—Magnetologic circuits are digital logic circuits constructed using magnetic tunnel junction (MTJ) devices. These devices are non-volatile, robust, and scale favorably with process dimensions. Several approaches exist for building magnetologic circuits. We are investigating current-mode magnetologic circuits as a viable option. Current-mode circuits avoid charging/discharging load capacitances and can be used to program a downstream device. Noise in a current-mode read circuit can affect the ability to correctly distinguish logic states in an MTJ. In this paper, we present a noise analysis of a current-mode read circuit or current conveyor. We derive analytical noise equations and verify them via simulation.

## I. INTRODUCTION

Thin-film magnetic devices based on the magnetic tunnel junction (MTJ) are actively being researched for applications in memory [1], field-programmable gate-arrays (FPGAs) [2], and logic computation [3]. Memory or Magnetic RAM (MRAM) circuits typically use current conveyors for readout of MRAM cells. FPGAs use unbalanced magnetic flip-flops in voltage-mode for configuration memory and registers. Logic circuits using these magnetic devices, called magnetologic, typically perform logic computation using voltage-mode sense amplifiers and H-bridge write circuits. The drawback to using voltage-mode in magnetologic circuits is that the charging/discharging of capacitances, such as capacitances due to wire-bonding MTJs, can result in slow operation.

The MTJ device, shown in Fig. 1, is constructed using two ferromagnetic layers separated by a thin insulator such as MgO [4]. The top ferromagnetic layer, called the free layer, can have a magnetic orientation in one of two directions. The bottom ferromagnetic layer, called the fixed layer, has its magnetic orientation in one direction because it is pinned during the manufacturing process. The resistance,  $R_{mtj}$ , as seen across the electrodes of the device, is dependent on the magnetic orientation of the free layer relative to the fixed layer. When the orientation of both layers is parallel (in the same direction), the resistance through the MTJ is low ( $R_L$ ). In contrast, when the orientation of both layers is anti-parallel (in opposite directions), the resistance through the MTJ is high ( $R_H$ ). Thus, the state is accessed as a resistance. A tunneling magnetoresistance ratio (TMR) is defined as  $TMR = \frac{R_H - R_L}{R_L}$ .

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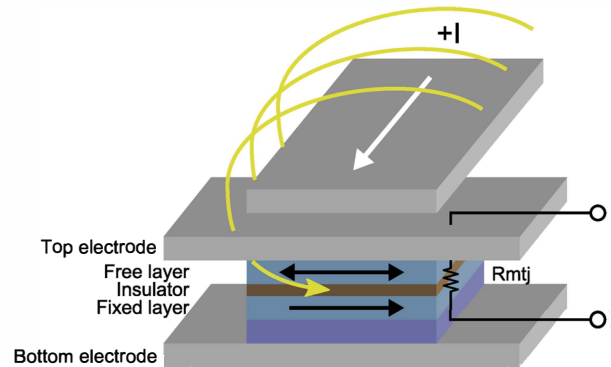


Fig. 1. A magnetic tunnel junction (MTJ) device that encodes state information in the magnetic orientation of the free layer. This state is programmed with a current (+I) and accessed as a resistance ( $R_{mtj}$ ) between the two electrodes.

that characterizes the separation between resistance states. The TMR is dependent on the bias voltage,  $V_{bias}$ , across the electrodes of the device. Large bias voltages result in small TMR and a high rate of device failure [4].

Two different writing approaches exist for programming the MTJ device: field-induced and spin-torque switching [4]. The device illustrated in Fig. 1 uses field-induced magnetic switching (FIMS), which is characterized by a conductor located a short distance from the tunnel junction and insulated from the top electrode. When current flows through the conductor, it induces a magnetic field which sets the magnetic orientation of the free layer. The spin-torque switching approach, in contrast, is programmed using a current that flows through the tunnel junction. In both writing approaches, the state of the MTJ is programmed with a current.

For magnetologic circuits, it is necessary to use CMOS integration to read the state of an MTJ device and to program a downstream device. We are investigating the use of current-mode read circuits for this purpose and plan to fabricate a prototype in a 3M2P 0.5  $\mu\text{m}$  process. The advantages are: 1) the output current can be used for programming the downstream device and 2) charging/discharging load capacitance associated with the MTJ is avoided which can lead to faster circuit operation.

A current-conveyor [5] is a current-mode circuit which can be used for reading the state of an MTJ device. It operates

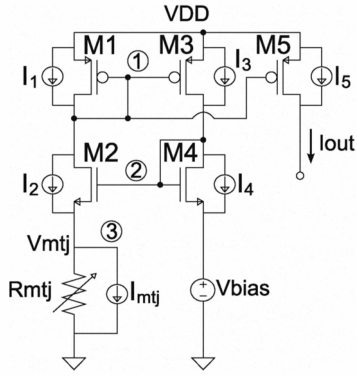


Fig. 2. Noise model of the current-mode read circuit for sensing MTJ resistance. Current sources,  $I_{1-5}$  and  $I_{mtj}$ , are added in parallel with transistors  $M_{1-5}$  and resistor  $R_{mtj}$  to model the noise contribution of each component, respectively. Circuit nodes 1 – 3, which are referred to in the analysis, are labeled with a circled number.

by clamping the voltage,  $V_{bias}$ , across the MTJ allowing the current  $I = \frac{V_{bias}}{R_{mtj}}$  to flow through the MTJ. This current is then mirrored to the output, optionally with amplification, in order to program a downstream MTJ.

Noise in the read circuit can affect the ability to correctly distinguish the logical state (0 or 1) of the MTJ device. It is therefore necessary to analyze circuit noise and to establish noise margins at the output for reliable operation.

A simple set of noise equations aimed at a broad family of circuits (both class A and AB current conveyors) were presented in [6] and then used to make qualitative conclusions. In this paper, we present a noise analysis of a class A current-conveyor circuit that is used for sensing the MTJ resistance. The resultant equations allow us to predict the output noise for the current-conveyor and use them as design equations for tuning circuit parameters to meet noise performance requirements. In Section II, the methodology employed in the noise analysis is given. In Section III, the noise analysis of the current-mode read circuit is described. In Section IV, the analytical expressions derived in the noise analysis are validated via simulation, and in Section V, general conclusions and future work are given.

## II. METHODOLOGY

The methodology used to perform the noise analysis of the current conveyor under consideration, shown in Fig. 2, involves several steps. The first step is to extend the circuit with current sources added in parallel with every transistor and resistor that models the noise current of these circuit components. The second step is then to construct a small-signal model of the circuit from which a frequency-independent DC transfer function,  $H_{dc,i}$ , is derived for each current source  $i$  to the output, making approximations as allowed to get a simplified form. The noise spectrum,  $S_i(f)$ , of each source is referred to the output,  $S_{out,i}(f)$ , by the equation

$$S_{out,i}(f) = |H_i(s)|^2 \cdot S_i(f) \quad (1)$$

where  $s = j2\pi f$ . At DC,  $S_{out,i}(0) = |H_{dc,i}|^2 S_i(0)$ .

TABLE I  
DC TRANSFER FUNCTIONS FROM NOISE SOURCE TO OUTPUT

$H_{dc,M1}$	$\frac{-1}{\frac{g_{m,n}}{g_{m,n}+g_{mtj}} + g_{mtj} \frac{g_{ds,n}+g_{sd,p}}{g_{m,n}+g_{mtj}} \left(\frac{1}{g_{m,n}} + \frac{1}{g_{m,p}}\right)}$
$H_{dc,M2}$	$\frac{1}{\frac{g_{m,n}}{g_{mtj}} + (g_{ds,n}+g_{sd,p}) \left(\frac{1}{g_{m,n}} + \frac{1}{g_{m,p}}\right)}$
$H_{dc,M3}$	$H_{dc,M2}$
$H_{dc,M4}$	$-H_{dc,M2}$
$H_{dc,M5}$	1 (exact)
$H_{dc,Rmtj}$	$\frac{1}{1+g_{mtj} \frac{g_{ds,n}+g_{sd,p}}{g_{m,n}} \left(\frac{1}{g_{m,n}} + \frac{1}{g_{m,p}}\right)}$

The third step is to determine the pole frequency,  $f_p$ , at each node which limits the bandwidth of the circuit and bounds the circuit noise. The pole frequency requires determining the resistance and capacitance seen at each node:

$$f_p = \frac{1}{2\pi R_{node} C_{node}} \quad (2)$$

The fourth step is to calculate the total integrated noise power,  $\overline{I_{out,i,n}^2}$ , of each source referred to the output:

$$\overline{I_{out,i,n}^2} = \int_{f=0}^{f=\infty} |H_i(s)|^2 S_i(f) df \quad (3)$$

There are two predominant noise spectra: thermal and  $1/f$  noise. We only consider thermal noise for simplicity in validating our results. Thermal noise has a flat noise spectrum independent of frequency and  $1/f$  noise has a spectrum with an inverse relationship to frequency. For a resistor, the thermal noise spectrum is  $S_{i,t} = \frac{4kT}{R} \left[\frac{A^2}{Hz}\right]$  [7], where  $k$  is Boltzmann's constant,  $T$  is the temperature, and  $R$  is the resistance. For a transistor, the thermal noise spectrum is  $S_{i,t} = 4kT\gamma g_m \left[\frac{A^2}{Hz}\right]$  [7], where  $\gamma$  is a coefficient that is typically equal to  $2/3$  for long-channel transistors, and  $g_m$  is the transconductance of the transistor.

The fifth step is to add all noise power contributions at the output to get the total noise power,  $\overline{I_{out,tot,n}^2}$ .

$$\overline{I_{out,tot,n}^2} = \sum_i \overline{I_{out,i,n}^2} \quad (4)$$

The square root of the noise power gives the standard deviation of the noise current present at the output.

## III. NOISE ANALYSIS

The current-mode read circuit used for sensing the resistance of an MTJ device, as shown in Fig. 2, is constructed using a current conveyor. The current conveyor ( $M_{1-4}$ ) clamps the voltage,  $V_{bias}$ , from the source of  $M_4$  to the source of  $M_2$  across the resistance,  $R_{mtj}$ . This voltage produces a current through  $R_{mtj}$  which is mirrored to the output using a current-mirror formed by  $M_1$  and  $M_5$  with unity gain. Each transistor is a current source operating in the saturation region.

The small-signal model of the current-mode read circuit was constructed with several simplifications. First, all NMOS transistors  $M_{2,4}$  have small signal parameters  $g_{m,n}$  and  $g_{ds,n}$ ,

TABLE II  
RESISTANCE AT EACH NODE

$R_1$	$\frac{g_{m,n}g_{m,p} + g_{mtj}g_{sd,p}}{g_{m,n} + g_{mtj}} + \frac{g_{m,p}}{g_{m,n}} + g_{ds,n} \left( \frac{g_{m,p} + g_{m,p} + g_{mtj}}{g_{m,n} + g_{mtj}} \right)$
$R_2$	$\frac{g_{m,n}^2}{g_{m,n} + g_{mtj}} + (g_{ds,n} + g_{sd,p}) \left( 1 + \frac{g_{m,n}g_{mtj}}{(g_{m,n} + g_{mtj})g_{m,p}} \right)$
$R_3$	$R_{mtj} \parallel \left( \frac{(g_{ds,n} + g_{sd,p})(g_{m,n} + g_{m,p})}{g_{m,p}g_{m,n}^2} \right)$

TABLE III  
CAPACITANCE AT EACH NODE

$C_1$	$C_{gs1} + C_{db1} + C_{db2} + C_{gd2} \left( 1 - \frac{V_{g2}}{V_{d2}} \right) + C_{gs3} + C_{gd3} \left( 1 - \frac{V_{d3}}{V_{g3}} \right) + C_{gs5} + C_{gd5}$
$C_2$	$C_{gd2} \left( 1 - \frac{V_{d2}}{V_{g2}} \right) + C_{gs2} \left( 1 - \frac{V_{s2}}{V_{g2}} \right) + C_{db4} + C_{gs4} + C_{db3} + C_{gd3} \left( 1 - \frac{V_{g3}}{V_{d3}} \right)$
$C_3$	$C_{mtj} + C_{sb2} + C_{gs2} \left( 1 - \frac{V_{g2}}{V_{s2}} \right)$

and all PMOS transistors  $M_{1,3,5}$  have small signal parameters  $g_{m,p}$  and  $g_{sd,p}$ , since the NMOS and PMOS transistors have the same aspect ratios  $\left(\frac{W}{L}\right)_n$  and  $\left(\frac{W}{L}\right)_p$ , respectively, and the same drain currents. Second, the bulk-modulation effect of transistor  $M_2$  is neglected. Third, the resistance  $R_{mtj}$  is represented as a conductance,  $g_{mtj} = \frac{1}{R_{mtj}}$ .

From the small-signal model, the DC transfer function of each noise source, modeled by current sources  $I_{1-5}$  and  $I_{mtj}$  in Fig. 2, to the output are presented in Table I. These can be simplified further (not shown) by assuming  $g_{mtj} \lesssim 4g_{m,n}$ . The transfer function is derived by considering one noise source at a time and calculating the current gain  $H_{dc,i} = \frac{I_{out}}{I_i}$  from that source to the output. The output noise spectrum is then referred to the output by (1) at DC.

Next, the pole frequencies are determined by deriving  $R$  and  $C$  at each node. The derived resistance equations for the current-mode read circuit are presented in Table II.

The capacitance seen at each node is determined by considering the gate-to-source ( $C_{gs}$ ), gate-to-drain ( $C_{gd}$ ), source-to-bulk ( $C_{sb}$ ), and drain-to-bulk ( $C_{db}$ ) capacitances of each transistor connected to the node and the capacitance associated with the MTJ ( $C_{mtj}$ ). The gate-to-bulk ( $C_{gb}$ ) capacitance is neglected because all transistors are operating in saturation. Capacitances that are connected to a small-signal ground are simply added together. Those capacitances that are coupled to other nodes are replaced with corresponding Miller capacitances [7]. For a prototype chip, wire-bond capacitance associated with the MTJ device is accounted for in  $C_{mtj}$  which is typically about 3 pF [7]. The derived capacitance equations are presented in Table III.

The pole frequencies are then calculated at each node and used to determine the effective bandwidth of the circuit. The system is then modeled as a 3-pole system, with the total

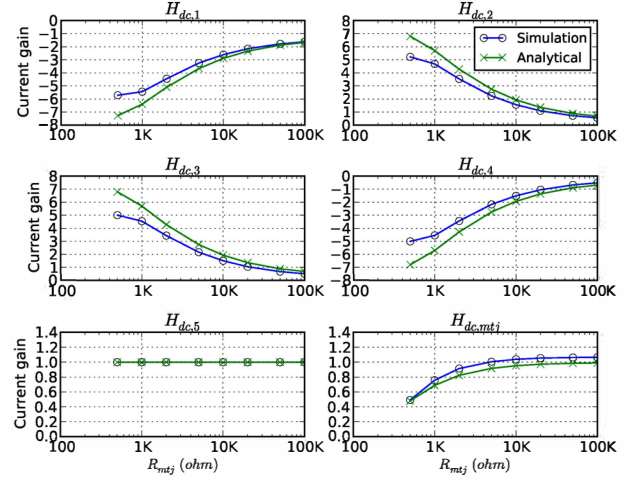


Fig. 3. DC transfer function validation with analytical and simulation results. Six plots are presented, one for each transfer equation,  $H_{1-5}$  and  $H_{mtj}$ , corresponding to the current gain from each current source to the output at DC. The X-axis shows the MTJ resistance,  $R_{mtj}$ , swept from 500  $\Omega$  to 100 k $\Omega$ . The Y-axis shows the current gain for simulation (blue with a  $\circ$ ) and analytical (green with an  $\times$ ) results.

integrated noise power for thermal noise,  $\overline{I_{out,i,nt}^2}$ , equal to

$$\overline{I_{out,i,nt}^2} = |H_{dc,i}|^2 \cdot S_{i,t} \cdot BW \cdot \frac{\pi}{2} \quad (5)$$

where the effective bandwidth,  $BW$ , is

$$BW = \frac{f_1 f_2 f_3 (f_1 + f_2 + f_3)}{(f_1 + f_2)(f_1 + f_3)(f_2 + f_3)} \quad (6)$$

#### IV. VALIDATION

We simulated the current-mode read circuit of Fig. 2 using a 3M2P 0.5  $\mu\text{m}$  process model to verify the equations derived in Section III. Small-signal parameters,  $g_m$  and  $g_{ds}$ , and capacitances  $C_{gs}$ ,  $C_{gd}$ ,  $C_{sb}$ , and  $C_{db}$  are extracted from the DC operating points of the circuit and used as parameters in the analytical expressions for the output noise. The noise of devices  $M_{1-5}$  and  $R_{mtj}$  are modeled with thermal noise only. In the equation of the thermal noise spectrum,  $S_t$ , of a transistor,  $\gamma = 1.0$  is chosen in agreement with simulation. The bias voltage,  $V_{bias}$ , across the MTJ is chosen to be 0.1 V in order to maintain a large TMR.  $R_{mtj} = 1$  k $\Omega$  unless specified otherwise.

##### A. DC Transfer Function Validation

The DC transfer functions in Table I are validated in Fig. 3 with analytical and simulation results. Simulation results are attained by measuring the current gain of current source,  $I_i$ , to the output in an AC analysis. The results are plotted versus the MTJ resistance,  $R_{mtj}$ , varied from 500  $\Omega$  to 100 k $\Omega$ . The six plots show the DC transfer function  $H_{dc,i}$  for each source. The analytical results were derived using first-order approximations which show the same trend as simulation and remain within 3 dB throughout the range of MTJ resistances.

TABLE IV  
ANALYTICAL CALCULATION OF POLE FREQUENCIES

Node	$R$	$C$	$f_p$
1	45.9 k $\Omega$	136 fF	25.5 MHz
2	51.8 k $\Omega$	48 fF	63.9 MHz
3	311 $\Omega$	3.28 pF	156 MHz

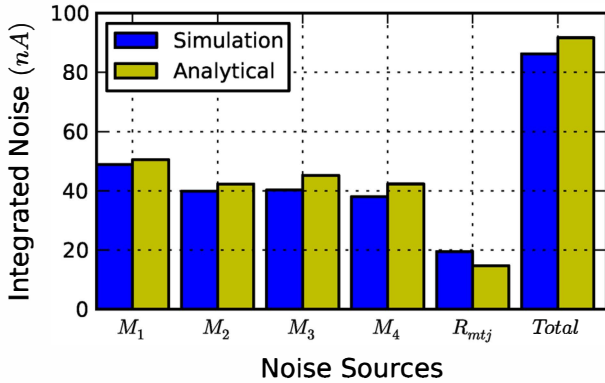


Fig. 4. Total integrated output noise validation with analytical and simulation results. The noise spectrum of each source referred to the output is integrated from 1 Hz to 1 GHz.

### B. Dominant Pole Validation

The dominant pole is the lowest frequency pole in the circuit. In simulation, we measured the dominant pole of the current-mode read circuit at the output to be 23.6 MHz. Analytically, we calculated resistance and capacitance seen at each node (assuming  $C_{mtj} = 3$  pF for wire-bond capacitance) and calculated each pole frequency,  $f_p$ , as shown in Table IV using (2). We found the lowest pole frequency to be 25.5 MHz. From (6), the effective bandwidth is calculated as 17.5 MHz.

### C. Total Integrated Output Noise Validation

The total integrated output noise is validated in Fig. 4 with analytical and simulation results. Analytical results are attained by calculating the thermal noise spectrum of each noise source, referring it to the output, and integrating the spectrum using (5). Simulation results are attained by measuring the total integrated noise of each noise source, modeled with thermal noise, from 1 Hz to 1 GHz. The noise contribution of  $M_5$  is not bounded because the current source  $I_5$  is connected directly in series with the output in the noise model. A downstream circuit will, however, bound this noise term. The total noise of all noise sources is computed using (4) and presented in the last column of the plot. The analytical results differ from the simulation results for two reasons. One, a higher DC current gain, except  $I_{mtj}$ , is predicted as compared to simulation giving an increase in the total integrated output noise. Two, a lower effective bandwidth is predicted as compared to simulation giving a decrease in the total integrated output noise. These two points counter each other, giving results that are within 2.5 dB of simulation for each noise source.

## V. CONCLUSION

This paper has provided a noise analysis of a current-mode read circuit for a magnetic tunnel junction device. The noise analysis presented here is only valid for nodes with low-pass transfer functions. The analytical expressions for noise at the output are validated against simulation results for the CMOS process we will be using for prototype fabrication.

While the numerical noise values presented in the simulation validation are limited to thermal noise for simplicity, the methodology generalizes for an arbitrary noise spectrum,  $S_i(f)$ . There are well known expressions for  $S_i(f)$  to model  $1/f$  noise, and as a general noise model becomes available for an MTJ device, it can be substituted for  $S_i(f)$  as well.

One of the uses of this type of noise analysis is to bound the operating points of the system in terms of a noise margin. With an MTJ resistance of  $R_H = 1$  k $\Omega$ , the read circuit will output a low current,  $I_L = \frac{V_{bias}}{R_H} = 100$   $\mu$ A, and with an MTJ resistance of  $R_L = 500$   $\Omega$ , the read circuit will output a high current,  $I_H = 200$   $\mu$ A. For this case,  $I_H - I_L \gg 10\sigma$ , which indicates that thermal noise in this circuit is not significantly limiting the noise margin. Note that noise margins must also take into account part-to-part variations and externally induced noise in addition to the internal noise analyzed here.

One of the advantages of current-mode operation is the relative insensitivity to load capacitance that might be present connecting the MTJ device to the CMOS circuit. While production fabrication is integrated, our prototype will use wire bonding. Due to the low impedance at node 3 in Fig. 2 (relative to node 1), parasitic capacitance of 1 to 5 pF will not significantly impact the noise performance or bandwidth of the circuit. This is consistent with node 1 rather than node 3 being the dominant pole in the circuit.

In addition to completing the physical prototype, our future work includes the analysis of a cascoded current conveyor, the transient analysis of current-mode read circuits both at 0.5  $\mu$ m and more aggressive technologies, and the exploration of differential read circuits (which use a complementary pair of MTJ devices to eliminate the need for an external reference).

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